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Wirebond crosstalk and cavity modes in large chip mounts for superconducting qubits

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Abstract

We analyze the performance of a microwave chip mount that uses wirebonds to connect the chip and mount grounds. A simple impedance ladder model predicts that transmission crosstalk between two feedlines falls off exponentially with distance at low frequencies, but rises to near unity above a resonance frequency set by the chip to ground capacitance. Using SPICE simulations and experimental measurements of a scale model, the basic predictions of the ladder model were verified. In particular, by decreasing the capacitance between the chip and box grounds, the resonance frequency increased and transmission decreased. This model then influenced the design of a new mount that improved the isolation to −65 dB at 6 GHz, even though the chip dimensions were increased to 1 cm × 1 cm, three times as large as our previous devices. We measured a coplanar resonator in this mount as preparation for larger qubit chips, and were able to identify cavity, slotline, and resonator modes.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

One promising approach toward quantum computation employs superconducting qubits [1]. Such qubits have been used to demonstrate simple gates [2–5] and quantum algorithms up to three qubits [6, 7]. As additional qubits are added, they will require increasing room on each chip, eventually necessitating a larger chip and increasing numbers of microwave control lines [8]. It will thus become crucial to carefully engineer the mounting box, both because the increased density of input lines could lead to greater microwave crosstalk between the lines, and because stray cavity modes, which can present new modes for dissipation [9], can appear with larger mounts.

For superconducting microwave devices such as qubits and kinetic inductance detectors [10], most chip mounts have placed or glued a chip onto a metal base [11–15]. Wirebonds are then used to connect the chip ground plane and pads to the external mount's ground plane and feedlines, which are typically made from a circuit board.

In this paper, we show that although such a mount may work well for the current generation of small chips, increasing the chip size will cause the ground connection to fail at microwave frequencies. Specifically, crosstalk will increase because of increased capacitance from the chip to mount ground, contrary to the usual assumption that tying the grounds together with capacitance improves their connection. With a simple ladder model, we explicitly show that this capacitance introduces a traveling wave mode between the chip and mount grounds, thereby giving a continuum of resonance modes which decouples the two grounds and provides a mechanism for large crosstalk.

To understand the effects from the wirebonds and mount, we first develop a semiquantitative model, and then discuss

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experimental tests using a simple scaled-up system. The predictions of this model were then used to design a new sample mount with a reduced capacitance between the mount and chip ground planes. An actual resonator device was then measured for this design. This mount accommodates a chip three times the area of our current generation of qubits; with this increase in size, and with added cavities to reduce the capacitances between the box and chip ground planes, we identified sources of cavity and chip modes up to 20 GHz.

2. Wirebond crosstalk

2.1. Circuit model

When mounting a microwave device, it is necessary to ensure that the chip is well grounded to the mounting box. This may be achieved using many short, closely spaced wirebonds around the edge of the die. To understand the effect of this network, we consider the simple model illustrated in figure 1, which will later be experimentally verified. Here, the grounding wirebonds between an input and an output feedline are considered to be an impedance ladder, with a node at each point where a wirebond connects to the chip ground plane.

Each wirebond can be modeled as a wire having inductance L_W between each node and the box ground. This inductance is proportional to the length of the wirebond, with a proportionality constant of approximately 1 nH mm^{-1} for typical wirebonds due to ground plane effects [16]. The length of the wirebond can be modeled to be approximately the minimum possible length for the wirebonds, the distance g between the chip and the edge of the mount. In addition, the edge of the chip ground plane gives an inductance L between two adjacent nodes. Its magnitude is $L = \ell d$ for an edge inductance per unit length ℓ and distance d between adjacent wirebonds. We assume the corresponding edge inductance from the mount ground plane is negligible because adjacent nodes are connected through the bulk. These two types of inductances give rise to a 'ladder model' for the interface between the chip and mount ground planes, as illustrated in figure 1(a).

We model microwave crosstalk as coming from voltage propagating along the ground nodes on the chip. The crosstalk between two ports can then be solved geometrically by following the approach [17] illustrated in figure 1(b), where the impedance looking into the ladder is given by Z and is independent of node position. The ratio of voltages between adjacent nodes of the inductor ladder is

$$\frac{V_1}{V_0} = \left[1 + \frac{\zeta}{2}\left(1 + \sqrt{1 + \frac{4}{\zeta}}\right)\right]^{-1} \quad (1)$$

$$\zeta = \frac{Z_1}{Z_2} = \frac{L}{L_W}. \quad (2)$$

As the inductance ratio L/L_W increases, the voltages along the nodes are more quickly suppressed. This implies that L_W should be reduced as much as possible by keeping wirebonds short. The voltage ratio between widely spaced points is given by a geometric sequence $V_n/V_0 = (V_1/V_0)^n$.

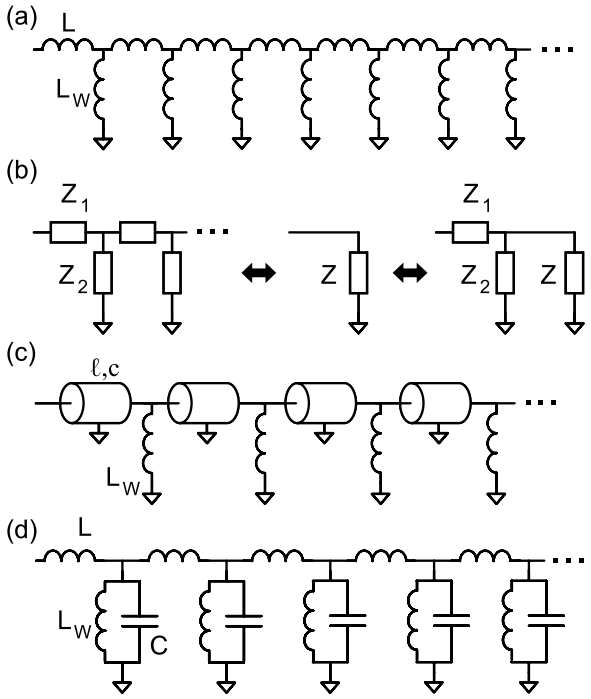

Figure 1. Ladder model of chip and wirebonds. (a) The chip ground plane and wirebonds are modeled as an inductor ladder. (b) A ladder with impedances Z_1 and Z_2 can be replaced by an effective impedance Z, or equivalently, by a single rung in parallel ($\|$) with the rest of the ladder, which is again equal to Z. Equating the latter two cases gives a quadratic equation for the effective impedance: $Z = Z_1 + (Z_2 \parallel Z)$. This can be solved for Z, and then the single rung is a voltage divider, giving $V_1/V_0 = (Z_2 \parallel Z)/(Z_1 + (Z_2 \parallel Z))$ [17]. (c) Schematic of the ladder model that incorporates the distributed nature of the edge inductance and ground capacitance. (d) Treating the ground capacitance as lumped elements adds a parallel impedance of opposite sign to the wirebond inductance, leading to an open circuit at the resonance frequency $f_{res} = 1/2\pi\sqrt{L_W C}$.

Note that while increasing the distance d between bonds increases L/L_W and thus reduces V_1/V_0, it also reduces the number of bonds n. As illustrated in figure 2, for increased attenuation it is more advantageous to have a high density of wirebonds than to space fewer wirebonds over the same length of ground plane.

Capacitance between the ground plane of the chip and the mount must also be included in the model. For a chip placed on a metal plane, this capacitance is distributed to all points on the ground plane of the chip, but for simplicity we treat it as being connected along the edge of the chip. This capacitance, along with the inductance L, is distributed over the length between wirebonds, giving a transmission line as illustrated in figure 1(c). By employing a π model [18], the capacitance can be divided between the wirebond nodes as lumped elements. As with parallel plate or coplanar capacitors, this capacitance C is proportional to the distance d between adjacent wirebonds, giving $C = cd$ for capacitance per unit length c. With these assumptions, the chip mount is represented by the model illustrated in figure 1(d), where capacitance is placed in parallel to the bondwire inductance. The ratio of voltages between adjacent nodes can be solved in

Table 1. Parameters for the scale model of the chip mount. The first three are measured from the model geometry: g is the gap between the ground plane and chip (the length of the bonds), d is the spacing between bonds, and *overlap* is the overlap distance between the chip ground plane (front side) and the mount ground plane (back). The capacitance c and inductance ℓ per unit length are calculated using COMSOL, while the remaining parameters are calculated from c and ℓ. The lumped element (LE) resonance frequency is given by $f_{\rm res} = 1/2\pi\sqrt{L_{\rm W}C}$ from the calculated inductance and capacitance. The transmission line (TL) resonance frequency is given by numerical evaluation of equation (4).

	g (mm)	d (mm)	Overlap (mm)	c (fF mm^{-1})	ℓ (nH mm^{-1})	L (nH)	$L_{\rm W}$ (nH)	$L/L_{\rm W}$	C (fF)	$f_{\rm res}$ (LE) (GHz)	$f_{\rm res}$ (TL) (GHz)
A	2.5	2.5	5.1	174.9	0.22	0.56	2.54	0.22	444	4.74	4.69
B	2.5	2.5	2.5	114.6	0.29	0.74	2.54	0.29	291	5.85	5.78
C	2.5	2.5	0.0	55.9	0.43	1.09	2.54	0.43	142	8.38	8.23
D	2.5	2.5	−2.5	32.4	0.58	1.47	2.54	0.58	82	11.0	10.75
E	2.5	5.1	2.5	114.6	0.29	1.47	2.54	0.58	582	4.14	4.04
F	2.5	1.3	2.5	114.6	0.29	0.37	2.54	0.15	145	8.28	8.23
G	5.1	2.5	2.5	114.0	0.30	0.76	5.08	0.15	290	4.15	4.12
H	1.3	2.5	2.5	117.2	0.28	0.71	1.27	0.56	298	8.18	8.00

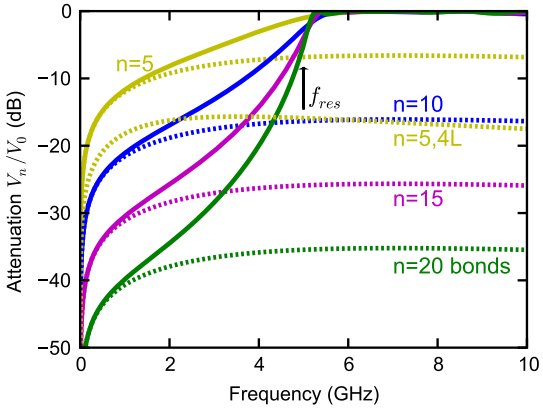

Figure 2. SPICE simulation of the ladder model. We plot voltage attenuation V_n/V_0 versus frequency for varying numbers of wirebonds $n = 5$ (yellow), 10 (blue), 15 (purple), and 20 (green). Dashed lines are for the inductor ladder, whereas the solid lines include capacitance. The parameters are similar to those in model A of table 1 for the 10× scale model, with $L = 0.5$ nH, $L_{\rm W} = 2.54$ nH, and $C = 0.4$ pF, giving $L/L_{\rm W} = 0.2$. We observe greater attenuation for increasing bond numbers both with and without capacitance. However, the transmission approaches unity above the resonant frequency of $f_{\rm res} = 1/2\pi\sqrt{L_{\rm W}C} = 5.0$ GHz when capacitance is included. The lower yellow dashed trace is for five bonds without capacitance, but with $L = 2$ nH to emulate the same distance as for the case of 20 bonds but with 1/4 the bond number; this result demonstrates the advantage of adding additional bonds rather than increasing the inductance ratio $L/L_{\rm W}$ with greater spacing.

the same manner as for (1), but here

$$\zeta = \frac{L}{L_{\rm w}} - \omega^2 LC. \tag{3}$$

When adding capacitance, the important result is that the wirebond inductance resonates with the capacitance at a frequency $f_{\rm res} = 1/2\pi\sqrt{L_{\rm W}C}$, resulting in a loss of shunting from the wirebonds. At (and above) this frequency, signals propagate along the chip ground without being strongly attenuated.

To account for the finite size of the ladder, we also simulated this circuit with SPICE [19] for various numbers of bonds and ratios of inductance and capacitance. These simulations confirmed quantitatively the predictions of the simple model, particularly that the transmission approaches unity above $f_{\rm res} = 1/2\pi\sqrt{L_{\rm W}C}$ and increasing numbers of bonds attenuate voltage more strongly at frequencies below the resonance. Figure 2 shows a typical simulation result, corresponding to model A of table 1.

We also checked the assumption of a lumped model for the ground inductance and capacitance by simulating short lengths of transmission lines, as illustrated in figure 1(c). By calculating the transmission matrix [20], we solved for the voltage ratios between nodes and found that the resonance frequency $\omega_0/2\pi$ satisfies

$$1 = \left(1 + \frac{\sqrt{\ell/c}}{2\omega_0 L_{\rm W}}\right)\cos(\omega_0 d\sqrt{\ell c}). \tag{4}$$

When solved numerically, we found predictions changed less than 5% as compared to the lumped model, indicating that the lumped model is adequate for the analysis presented here.

2.2. Experimental setup and analysis

To verify semiquantitatively the predictions of this ladder model, we built a scale model of a chip, its wirebonds, and a mount, as illustrated in figure 3. The scale models were commercially fabricated on FR-4 circuit board with double sided-copper and plated vias. The effects of capacitance from the chip to the mount were modeled by varying amounts of metal overlap between the top and bottom sides of the board. We assumed that the wirebond inductance scaled as 1 nH mm^{-1} multiplied by the gap between the two ground planes, and that the edge inductance and capacitance scaled as the distance between adjacent wirebonds.

On the top side, the chip was modeled by a 64 mm metal square, ten times larger than our group's standard qubit chips. A gap of width g separated this ground plane from that of the mount ground. Stretching across the gap were 0.25 mm wide metal traces that simulated the wirebonds. To measure the voltage attenuation down the chip, we included three signal leads, separated by 13 and 23 mm, that were connected by a coplanar waveguide to a 50 Ω resistor placed across the gap to the chip ground plane. The ground plane on the back side of the circuit board was connected with vias to the ground plane of the top mount. While there are two propagation paths available

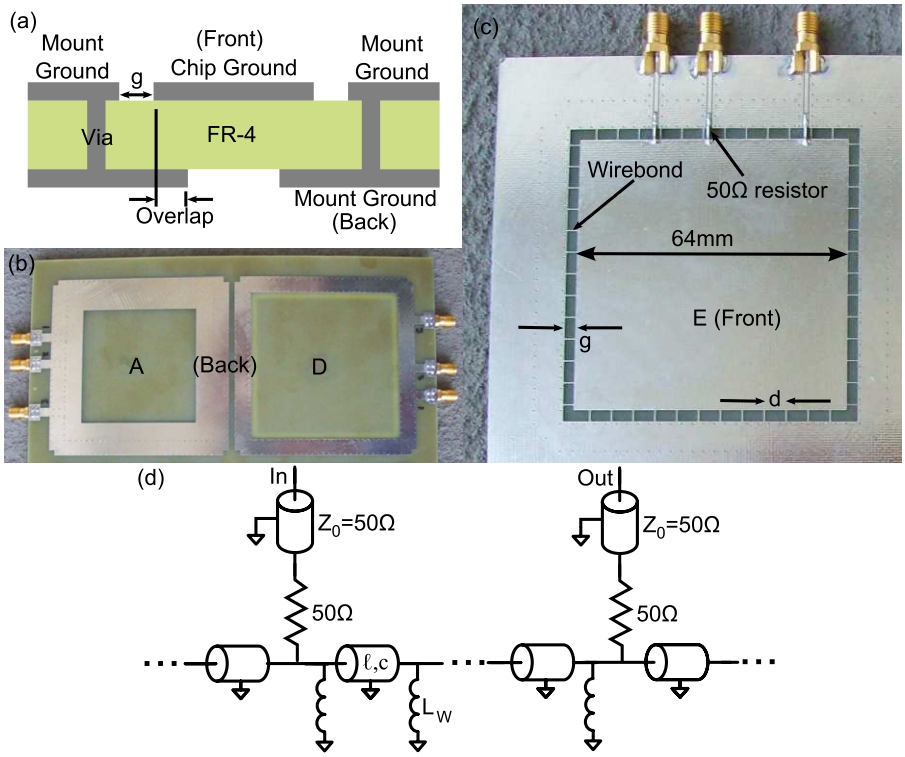

Figure 3. Scale model of the chip mount. Each model is 64 mm wide and high, which is ten times larger than our standard chips. (a) Cross-section view (not to scale). The model consists of a chip ground (the center square on the front side) and two chip mount grounds (the two hollow squares on both the front and back sides), where the chip mount grounds are connected through vias. A gap in the front side models the separation between the chip and mount grounds. (b) Views of the back of panels (A) and (D) demonstrate varying overlaps of the mount ground plane and the chip ground. (c) Front side view of panel (E). Each model has three microwave ports, connected to the chip ground via a 50 Ω resistor, so that transmission can be measured for separation distances 13, 23, and 36 mm. Wirebonds are modeled by traces 0.25 mm wide connecting the chip and mount grounds. (d) Schematic of the scale model, showing 50 Ω ports and resistors.

between any two ports, the one consisting of three sides of the square is 6–19 times longer than the shorter path. As shown by figure 2, the longer path is thus negligible compared to the shorter one.

As illustrated in table 1, we used a default distance of 2.5 mm for the gap between the front and back side ground planes, the distance between adjacent bonds, and the overlap distance between the front side chip and the back side ground plane. These three parameters were changed for the eight different models. For each model, the COMSOL multiphysics package [21] was used to calculate the edge inductance and capacitance per unit length; these parameters, along with the inductances and capacitances derived from these values, are also included in table 1.

We used a vector network analyzer at room temperature to measure the scattering matrix for these scale models. By measuring S_{21} between pairs of the three connectors, we were able to determine attenuation for three different lengths. The resulting traces are shown in figure 4.

As predicted by the frequency dependence of the model, we observed rolloff at very low frequency, then rising transmission until a resonance frequency, after which the transmission remains high. Below the resonance frequency, we observed increased attenuation for increased number of wirebonds, with frequency dependence and magnitudes in qualitative agreement with theory. Loss from the circuit board was important above approximately 5 GHz, as expected for an FR-4 substrate and copper metallization. The predicted resonance frequency f_{res} is shown as a vertical black line in all plots, which shows reasonable agreement between experiment and theory.

Panels (A)–(D) show that the resonance frequency f_{res} increases with decreasing ground capacitance, as expected by theory. Changing the wirebond spacing (panels (E) and (F)) and wirebond length (panels (G) and (H)) shows a change in frequency in the correct direction. The change is smaller than predicted for panels (F) and (H), probably due to mutual inductance between the bonds.

With some confidence in the basic model, it is possible to extract useful information about practical design issues, such as the effect of nonuniform wirebonding, which occurs as a result of unsuccessful wirebonds. Using SPICE simulations, we modeled a gap in the wirebonds with an increased inductance L and capacitance C at one location in the ladder. Surprisingly, the lower-frequency resonance at this one location produces transmission through the entire ladder, leading to a peak in the transmission as seen in figure 5. This indicates that wirebonds should be made as uniformly as possible all the way around the chip. However, note that even with a gap of 10 bond spacings, the resonance frequency is only reduced by a factor of two. For the case of long wirebonds, the resonance frequency is lowered at one spot

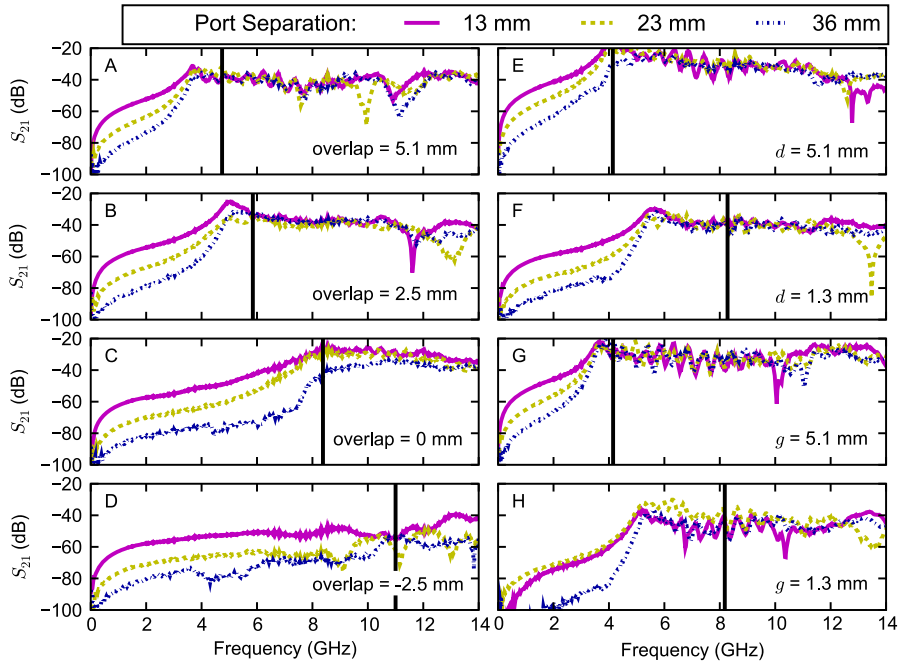

Figure 4. Transmission versus frequency measured in 10× scale models. Scaling implies frequencies would be ten times larger for 6 mm chips. Data are plotted for three distances: 13 mm (magenta solid), 23 mm (yellow dashed), and 36 mm (blue dash-dot). At low frequency, the data show small transmission that increases with fewer wirebonds. The transmission increases with frequency and peaks at a resonance frequency that is in qualitative agreement with the theoretical model. Panels (A)–(D) show a systematic increase in resonance frequency for decreasing chip capacitance to ground, which is in reasonable agreement with the prediction of $f_{\rm res}$ indicated by the black vertical line. The decrease in transmission at high frequencies is due to dissipation in the FR-4 and copper. Panels (E) and (F) show changes from the spacing d between wirebonds, indicating that longer (shorter) spacing produces a smaller (larger) resonance frequency, as expected. Panels (G) and (H) show dependence on wirebond length g, which again changes the resonance frequency and low-frequency transmission in the predicted direction. Differences between the experimental and predicted $f_{\rm res}$, particularly in panels (F) and (H), are probably due to mutual inductance between the bonds, which has not been included in the model.

in the ladder, but does not lead to a significantly lowered resonance in the transmission. In contrast, increasing the capacitance locally does lower the resonance frequency. In summary, small irregularities in wirebonding do not appear to be critical to the mount performance.

3. Mount for large chips

We used this model to design a new mount and to calculate its expected performance. To determine the effects of wirebond spacing and length, COMSOL was used to calculate the inductance and capacitance for a mount with different wirebond configurations. We assumed the mount had ground planes 1.4 mm above and 1.9 mm below the chip. We considered the effect of various bond spacings with a gap between the box and chip ground plane of 200 μm and a bond length of 400 μm, which accounts for the arching of the bond. For a bond spacing of 500 μm, giving a total of 20 bonds per cm, we calculated $f_{\rm res} = 43$ GHz and $L/L_{\rm W} = 0.37$, for an attenuation of 5.2 dB per bond (104 dB cm^{-1}). A bond spacing of 200 μm, for a total of 50 bonds per cm, gives $f_{\rm res} = 68$ GHz and $L/L_{\rm W} = 0.15$, and an attenuation of 3.3 dB per bond (167 dB cm^{-1}). These results show that acceptable attenuation is possible using parameters that are experimentally feasible.

A new mount was designed for chips with 1 cm sides to achieve these wirebonding parameters and to experimentally test performance. As illustrated in figure 6, we used many short wirebonds between the chip and the mount to reduce crosstalk. Stray capacitance was minimized by designing a box with cavities both above and below the chip. The box was made from aluminum to shield stray magnetic fields when the devices are cooled to temperatures below 100 mK.

We used a coplanar resonator chip to quantify the mount performance. The resonators were optically patterned 150 nm thick aluminum films sputtered on silicon. The chip mount was cooled by an adiabatic demagnetization refrigerator to approximately 100 mK. The results from resonator measurements are plotted in figure 7, which have the transmission magnitudes normalized by removing cable attenuation in order to express the results as a mount response.

As illustrated in figure 7(a), we measured a transmission of −65 dB at 6 GHz, only somewhat larger than coming from open-circuit transmission without the mount. The noise in the data comes from the noise floor of the network analyzer.

4. Identification of spurious modes

As shown in figure 7(b.1), we observed several resonance modes when the chip was measured at 100 mK. This is partly due to the large size of the mount, which has dimensions of 1 cm, approximately a half-wavelength for the highest

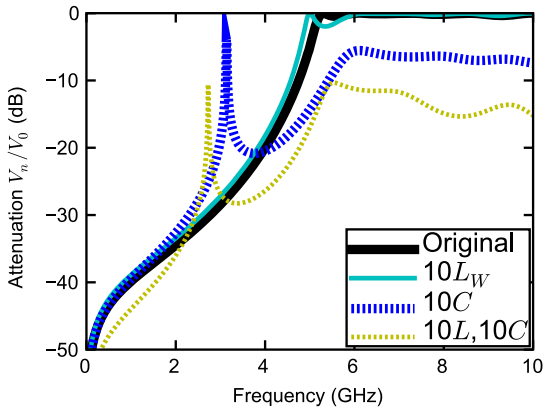

Figure 5. SPICE simulation of nonuniformity in the ladder model. Parameters used are identical to figure 2 with 20 bonds, but with a change in L and C for one bond halfway down the line. The thick solid black trace is for an unchanged ladder, as in figure 2. The thin dashed yellow trace corresponds to increasing both L and C by a factor of ten to simulate a single gap lengthened by a factor of ten. For the thick dashed blue trace, C is increased ten-fold to simulate unwanted capacitance with no gap in bonds. Finally, the solid cyan trace is for a ten-fold increase in L_W to simulate a bond that is much too long. While the discontinuities in capacitance lead to resonant transmission at low frequencies, an increased wirebond inductance does not, indicating that the grounding performance is less sensitive to irregularities in the wirebonds themselves.

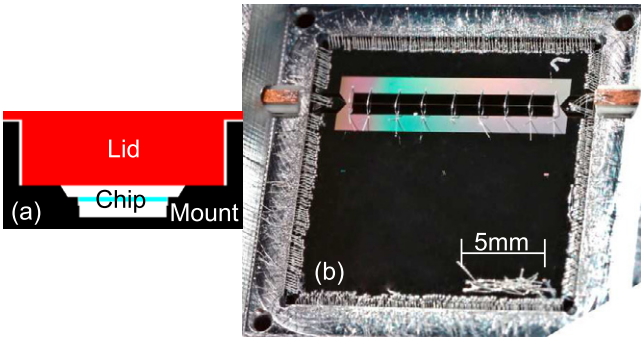

Figure 6. Design of the chip mount. (a) Cross-sectional view of the mount, showing the main aluminum box (black), chip (cyan), and lid (red). To raise f_{res}, we use cavities above and below the chip with height 1.4 mm and 1.9 mm, respectively. (b) Photo of chip in mount, showing numerous small wirebonds to ground around the edge of the chip to suppress crosstalk. The wirebond spacing and length are approximately 0.13 mm and 0.7 mm, respectively. This chip has a coplanar resonator between two central pads, with wirebonds bridging the resonator to suppress slotline modes.

frequencies studied here. In order to identify the modes, we performed several additional experiments.

One test was to measure the resonator at room temperature, as shown in figures 7(b.3) and (b.4). The presence of resonance modes at 16 GHz and at 19.6 GHz indicates these are cavity modes, as the lack of superconductivity precludes a chip resonance mode. As a further test, we then either removed the lid (see figure 7(b.2)) or placed Eccosorb LS-26 microwave-absorbing foam inside the sample mount lid (data not shown), and observed the disappearance of the 16 GHz resonance, leaving only the 19.6 GHz peak. We interpret this as the 16 GHz peak coming from a cavity resonance between the chip and mount lid. The 19.6 GHz peak probably comes from the smaller cavity below the chip.

Slotline modes are another source of undesirable resonances, which correspond to having unequal voltages on the ground planes on either side of the coplanar resonator. To identify these modes, a resonator chip was fabricated the same as the coplanar resonator but with no center trace; these measurements are plotted in figure 7(b.5), where we find resonance modes at 8.1, 13.6, and 20 GHz. Since these have not previously been identified as cavity modes, we identify them as slotline modes. Note that their frequency ratios are close, but not equal, to 1:2:3. These modes may be suppressed by airbridge wiring spanning the coplanar leads, which forces the voltages on either side to be equal. As illustrated in figure 6, we emulated this by spanning all coplanar traces with about 30 wirebonds, although we later found that nine wirebonds

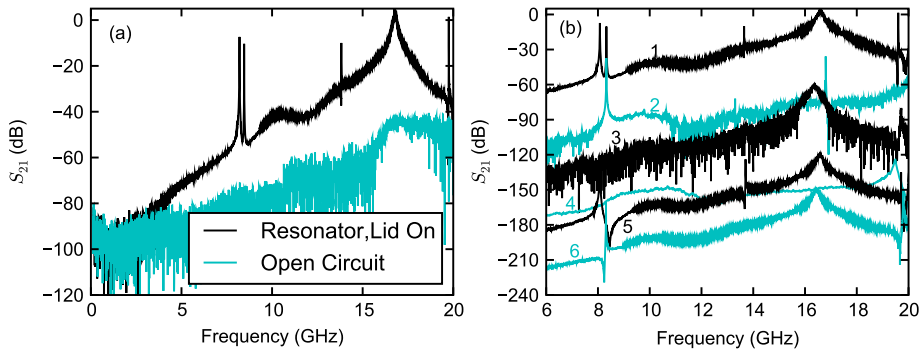

Figure 7. Identification of resonance modes. (a) Plot of mount transmission S_{21} versus frequency for a coplanar resonator (black) and an open circuit without the mount (cyan), measured at 100 mK. The crosstalk is found to be −65 dB at 6 GHz, and somewhat less without the chip. (b) Expanded scale of transmission showing major resonances, which can be identified by various test experiments. Additional cases are each displaced by 30 dB from each other for clarity. Case 1 is for the chip data in (a), and 2 is for the resonator with the lid off. Cases 3 and 4 are taken at room temperature, with the lid on and off, respectively. These four cases identify the cavity modes at 16 and 19.6 GHz. Case 5 is for an identical chip design but with the center conductor removed, and 6 is for the original chip (case 1) after adding wirebonds that bridge the slotline gap. The suppression of resonances with these shorts identifies the slotline modes at 8.1, 13.6, and 20 GHz. The remaining two modes, at 8.4 and 16.7 GHz, are the resonator modes. Some peaks consist of both a peak and a dip due to interference between stray transmission and the resonance mode.

sufficed. When doing so, we found these three slotline modes were all suppressed, as shown in figure 7(b.6).

We identify the mode at 8.4 GHz as the coplanar resonator mode, since it is not a cavity or slotline mode. This matches the design value of about 9 GHz. This was further confirmed by cooling through the transition temperature while applying a 2.5 G magnetic field; as this value exceeds the critical field for the 6 μm width traces for flux trapping [22], one expects a significant decrease in the Q factor [23, 24]. By following the approach in [25] for measuring Q, we found this mode dropped in Q by a factor of ten, whereas other modes were only degraded by at most a factor of two. We also found the characteristic field size for degradation of Q was consistent with the width of the resonator's center trace.

Finally, when the lid was removed, an additional resonance mode was present at 16.7 GHz, as shown in figure 7(b.2). With the lid attached, the 16 GHz cavity mode had masked this additional mode. The Q for this mode decreased by more than a factor of ten with field cooling, implying this is a coplanar mode. This is consistent with expectations since the frequency of this mode is almost twice that of the fundamental coplanar mode.

We note that increasing the chip size beyond 1.5 cm will lower the frequency of cavity modes to that near the qubit, an issue that will clearly have to be addressed in future research. Since we observed that damping reduces cavity crosstalk in figure 7(b.4), we expect that efficient damping of these modes will enable the construction of large chip mounts with low crosstalk. It is also likely that using simulation programs to model the mount will enable further reduction of these modes [26].

5. Conclusion

In conclusion, we have modeled crosstalk in a microwave chip mount as arising from non-zero wirebond inductance. An impedance ladder model has been developed that can predict the performance on the grounding and was experimentally verified with a scale model. Our calculations indicate that stray transmission falls off at low frequencies with increasing wirebond density, and reaches near unity at a resonance frequency determined by the wirebond length and the stray capacitance between the chip and mount grounds. Hence, to improve the mount, it is necessary to use a high density of short grounding wirebonds and to decrease stray capacitance by using a mount without a ground plane under the chip.

A new chip mount was developed with this improved design in mind. We were able to characterize various resonances, including coplanar, cavity, and slotline modes. The stray coupling was reduced to about -65 dB at 6 GHz. This new mount is compatible with centimeter-sized chips for future qubit devices and points the way for even larger chip sizes.

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